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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,603	06/28/2001	Yoshihiko Toyoda	401265	4828

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,603	TOYODA, YOSHIHIKO	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13* is/are pending in the application.

4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. The amendment filed on 03/11/2003, paper no. 10 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-10 and 13.

Election/Restrictions

2. Applicant's election of Group species 1, which encompass generic claim 1 and dependent claims 2-5, and in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 01/1/2001. The certified copy of the priority document has been received.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 5,960,317) in view of Onoda (US 5,905,305).

6. Regarding claim 1, Jeong (e.g. fig. 3c) shows a semiconductor device comprising an insulating layer (57 and 59a) having an outside surface and including a plurality of grooves (e.g. 58) having different widths, each of the grooves including side surface and bottom surface, at least one of the grooves including a plurality of recesses extending entirely within the insulating layer, from the bottom surface of the groove, and into the insulating layer; and a conductive layer 63a filling each of the grooves and other recesses, the conducive layer include a layer 61a covering the side surfaces of the grooves and internal surfaces of the recesses. Although Jeong does not explicitly depict that the grooves includes a plurality of recesses it is well known in the art that this type of interconnection includes plurality of recesses or hole contacts. Those skilled in the art will understand that wiring 50 is interconnected by a plurality of contacts holes in the direction perpendicular to the cross-sectional view shown in figure 3c (depth). Note that plural contact holes are required in order to interconnect different wiring levels. For example, Onoda figure 3 shows a typical interconnection arrangement that includes a wiring layer and a plurality of recesses. In this case, Onoda shows a wiring layer 102 (which equates to Jeong's layer 50) having a plurality of connections 104 (which equate to the Jeong's connections 58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of recesses in the Jeong's device in a direction perpendicular to the cross section al view as that taught by Onoda

since it is well known in the art that wiring layers are connected with a plurality of vias in order to interconnect the different wiring levels.

7. Regarding claim 13, Jeong shows that the surface and the bottom surface of the grooves are traversed and parallel to the outside surface of the insulating layer, respectively.

8. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 5,960,317) in view of in view of Onoda (US 5,905,305) further in view of Jeng et al. (US 5,893,734

9. Regarding claim 2, Jeong in view of Onoda shows most aspects of the instant invention including a non-planar bottom surface having an aspect ratio (i.e. depth to width ratio). Jeong in view of Onoda does not disclose the specific the depth to width ratio. Jeng discloses that the aspect ratio of electrical interconnections is subject to optimization. According to Jeng, high aspect ratios make more difficult the size reduction of semiconductor devices. Therefore, it is desirable to minimize the aspect ratios of the multilevel contacts holes during the downscaling of the minimum feature sizes of the devices (col. 1/lls. 9-67 and col. 2lls. 1-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the depth to width ratio and/or to optimize the aspect ratio of the grooves disclosed by Jeong in view of Onoda in view of Onoda in order to effectively reduce the overall device size as suggested by Jeng. With regards to the specific aspect ratio claimed by applicant, i.e., a ratio of depth to width of not more than 0.7, is only considered to be the "optimum" depth to width ratio of the opening disclosed by the Prior Art that a person having

ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as filled groove is used as already suggested by the Prior Art.

10. Regarding claim 3, Jeong in view of Onoda shows most aspects of the instant invention including a non-planar bottom surface having an aspect ratio (i.e. depth to width ratio). Jeong in view of Onoda does not disclose the specific the depth to width ratio. Jeng discloses that the aspect ratio of electrical interconnections is subject to optimization. According to Jeng, high aspect ratios make more difficult the size reduction of semiconductor devices. Therefore, it is desirable to minimize the aspect ratios of the multilevel contacts holes during the downscaling of the minimum feature sizes of the devices (col. 1/lls. 9-67 and col. 2lls. 1-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the depth to width ratio and/or to optimize the aspect ratio of the grooves disclosed by Jeong in view of Onoda in order to effectively reduce the overall device size as suggested by Jeng. With regards to the specific aspect ratio claimed by applicant, i.e., a ratio of depth to width of not more than 0.35, is only considered to be the "optimum" depth to width ratio of the opening disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In

re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as filled groove is used as already suggested by the Prior Art.

11. Regarding claim 4, Jeong in view of Onoda shows most aspects of the instant invention including a non-planar bottom surface having concave portion 60 with a groove shape. Also, the concave portion has an aspect ratio (i.e. depth to width ratio). Jeong in view of Onoda does not disclose the specific the depth to width ratio. Jeng discloses that the aspect ratio of electrical interconnections is subject to optimization. According to Jeng, high aspect ratios make more difficult the size reduction of semiconductor devices. Therefore, it is desirable to minimize the aspect ratios of the multilevel contacts holes during the downscaling of the minimum feature sizes of the devices (col. 1/lls. 9-67 and col. 2lls. 1-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the depth to width ratio and/or to optimize the aspect ratio of the grooves disclosed by Jeong in view of Onoda in order to effectively reduce the overall device size as suggested by Jeng. With regards to the specific aspect ratio claimed by applicant, i.e., a ratio of depth to width greater than 0.35, is only considered to be the "optimum" depth to width ratio of the opening disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results,

i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as filled groove is used as already suggested by the Prior Art.

12. Regarding claim 5, Jeong in view of Onoda shows most aspects of the instant invention including a non-planar bottom surface having concave portion 60 with a groove shape. Also, the concave portion has an aspect ratio (i.e. depth to width ratio). Jeong in view of Onoda does not disclose the specific the depth to width ratio. Jeng discloses that the aspect ratio of electrical interconnections is subject to optimization. According to Jeng, high aspect ratios make more difficult the size reduction of semiconductor devices. Therefore, it is desirable to minimize the aspect ratios of the multilevel contacts holes during the downscaling of the minimum feature sizes of the devices (col. 1/lls. 9-67 and col. 2lls. 1-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the depth to width ratio and/or to optimize the aspect ratio of the grooves disclosed by Jeong in view of Onoda in order to effectively reduce the overall device size as suggested by Jeng. With regards to the specific aspect ratio claimed by applicant, i.e., a ratio of depth to width greater than 0.7, is only considered to be the "optimum" depth to width ratio of the opening disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as filled groove is used as already suggested by the Prior Art.

Response to Arguments

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Applicant argues that the prior art does not disclose grooves confined within an insulating layer having a plurality of recesses (new limitation). Nonetheless, Jeong (e.g. fig. 3C) clearly shows that the grooves (e.g. 58) are confined within the insulating layer (57 and 59a). Moreover, it is well known in the art that wiring layers are connected by a plurality of recesses (see paragraph 6).

14. Applicant argues that the optimization referred to in Jeng pertains to making electrical contacts, no to filling interconnection grooves with a metal so that interconnection grooves of different width are essentially uniformly filled. This argument is not persuasive since the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Moreover, as stated in the previous action this limitation is recognized as a result-effective variable. Therefore, a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)). Finally, Applicant fails provide evidence regarding non-obvious nor unexpected results.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

18. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

19. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/502, 758, 773 and 775	05/03
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	05/03

Leonardo Andújar
Patent Examiner Art Unit 2826
LA
5/19/03